**Experiment No. 3**

**Title: Design of digital system using Multiplexer.**

**Batch: A3 Roll No.: 16010421075 Experiment No.: 3**

**Aim:** Design of digital system using a Multiplexer

**Resources needed:** Circuitverse online simulator or Hardware kit

**Theory:**

Multiplexer also called Data selector. A digital circuit which selects one of the 2*n* data

inputs and route it to the single output. Select lines are(n) and Input lines are (2n)

.

D0

D1

S0

Q

Input 0

Input 1

Select

Input

fig 1. A 2 : 1 multiplexer

In this case there are two input terminals D0 and D1, one select input S0 and one output Q. When the select input is set to logic 0, D0 is connected to the output. When the select input is set to logic 1, D1 is connected to the output Q.

D0

D1

S1

Q

Input 0

Input 1

Select

Inputs

D2

D3

Input 2

Input 3

S0

**Fig 2**. A 4 : 1 multiplexer.

In this case there are four data input terminals D0 – D3, two select inputs S0 and S1 and just one output Q. The following truth table shows when each of the data inputs is connected to the output.

|  |  |  |
| --- | --- | --- |
| **Select Inputs** | | **Output** |
| **S1** | **S0** | **Q** |
| 0 | 0 | D0 |
| 0 | 1 | D1 |
| 1 | 0 | D2 |
| 1 | 1 | D3 |

**Table1**. Truth table for 4:1 multiplexer

D0

D1

S1

Q

Input 0

Select

Inputs

D2

D3

Input 7

S0

S2

D4

D5

D6

D7

fig 3. An 8 : 1 multiplexer.

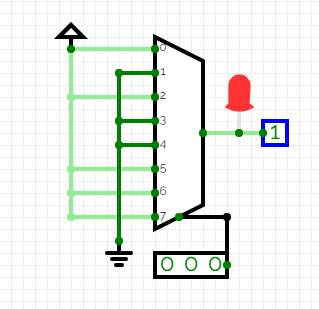
|  |  |  |  |
| --- | --- | --- | --- |
| **Select Inputs** | | | **Output** |
| **S2** | **S1** | **S0** | **Q** |
| 0 | 0 | 0 | D0 |
| 0 | 0 | 1 | D1 |
| 0 | 1 | 0 | D2 |
| 0 | 1 | 1 | D3 |
| 1 | 0 | 0 | D4 |
| 1 | 0 | 1 | D5 |
| 1 | 1 | 0 | D6 |
| 1 | 1 | 1 | D7 |

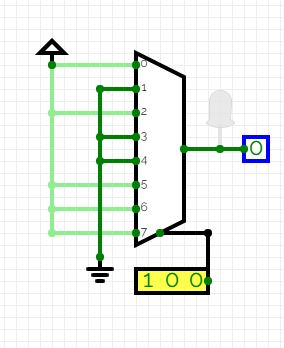
**Table2**. Truth Table for 8:1 Multiplexer

* The above truth table shows when the data inputs are connected to the output.
* Multiplexers are commonly used in communication systems; however they can be used in Logic System design and simplification as well.

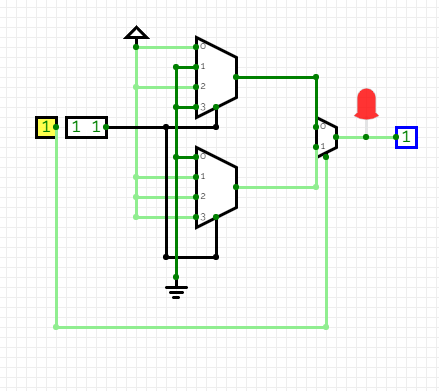
**Exercise 1**: Show how an 8**:**1 multiplexer can be used to implement the logic function given below:-

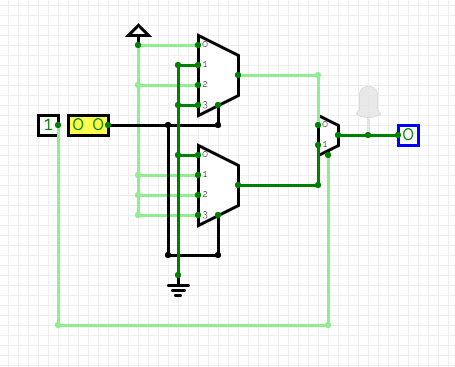
**F (A, B, C) = ∑m (0, 2, 5,6, 7)**





**Exercise 2**: Solve the above problem using two 4:1 multiplexers.





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**Procedure**:

1. Design logic circuits for given examples.
2. Simulate / Connect the circuit for both cases and verify the outputs.
3. Upload the write-up with the solved design problems given in write-up.

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**Observations and Results:** Solve the examples as given in write-up/given during Lab session and Simulate as per instructions in Lab session

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**Outcomes:**

**CO 2: Understand the basic building blocks, techniques used in digital logic design.**

**CO 3: Design the combinational and sequential circuits using basic building blocks.**

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**Conclusion:**

An 8:1 multiplexer consists of eight data inputs D0 through D7, three input select lines S0 through S2 and a single output line Y. Depending on the select lines combinations, multiplexer selects the inputs.

Using the above concept we did a virtual representation of an 8:1 multiplexer.

Similarly we converted an 8:1 to 4:1 using 2 4:1 multiplexers and 1 2:1 multiplexer and got the result. And printed the outcomes above.

**Grade: AA / AB / BB / BC / CC / CD /DD**

**Signature of faculty in-charge with date**

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**References:**

**Books/ Journals/ Websites:**

1. R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill.